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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,472	08/29/2001	Katsuji Kimura	Q65962	4891

7590 08/25/2003

SUGHRUE, MION, ZINN, MACPEAK & SEAS
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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/940,472	Applicant(s) KIMURA, KATSUJI	
	Examiner Minh Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/28/03 has been entered.

Claim Objections

2. Claims 1 and 3 are objected to because of the following informalities:

In claim 1, line 3, "two input voltage" should be changed to -- two input voltages --,

lines 10-11, "half an output voltage" should be changed to -- an addition output voltage -- to be consistent with the term used on line 2 of claim 2.

In claim 3, line 2, "firs" should be changed to -- first --,

lines 4-5, "a signal to be subtracted" should be changed to -- signals to be subtracted -- to avoid misdescriptive problem since the drain of the first MOS transistor outputs one signal and the drain of the second MOS transistor outputs another signal, i.e., there are more than one signals.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 3-4 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,602,509, issued to Kimura.

As per claim 3, Kimura discloses a voltage adder/adder circuit (Fig. 3) comprising:

a differential pair (1) having a first MOS transistor M1 and a second MOS transistor M2, wherein the gate electrodes of the first and second MOS transistors forming input terminals, i.e., the gate terminals of M1 and M2, for receiving an input differential voltage (Vi), the drain electrodes forming output terminals to the subtractor circuit (3) for outputting signals (ID1 and ID2) to be subtracted by the subtractor (3), and source electrodes of M1 and M2 commonly coupled to form an output terminal (the common source node) for outputting a voltage to be added (the voltage at the common source node); and

a constant current source (the source which provides the current I shown in box 2, also see column 2, line 21) which drives the differential pair (1).

As per claim 4, using a level shifter to shift the voltage at the common source node of an adder circuit is taught by Kimura in column 2, lines 51-55 (Fig. 1, transistors M55).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,602,509, issued to Kimura.

As per claim 1, Kimura discloses a voltage subtract or/adder circuit (Fig. 3) comprising:

a current subtractor (3) for providing an output terminal for outputting an output current delta(I) in proportion to the subtraction of two input voltages (one is at the gate of M1 and the other one is at the gate of M2);

a differential pair (1) having a first MOS transistor M1 and a second MOS transistor M2, wherein the gate electrodes of the first and second MOS transistors forming input terminals for receiving the input voltages (the input voltages at the gates of M1 and M2), the drain electrodes of the first and second MOS transistors supplying a differential current to the current subtractor (the ID1 and ID2 currents) to the subtractor (3), and source electrodes of M1 and M2 coupled to form an output terminal for outputting an addition output voltage in proportion to the addition of the two input voltages (see the formula in box 2); and

the sum of currents flowing through the M1 and M2 increases in proportion to the square of a difference of the two input voltages (see the formula shown in box 2, Vi^2 term).

Kimura does not explicitly disclose a current to voltage converting means for providing an output voltage in proportion to the subtraction of two input voltages as called for in the claim.

The Examiner takes Official Notice the fact that using a resistor to convert a current into voltage is old and well known in the art, i.e., using Ohm's Law, V=RI, and the practice is well-known in the electronic field.

It would have been obvious to one skilled in the art at the time of the invention was made to connect a resistor to the output of the subtractor circuit (3) in the Kimura circuit shown in Fig. 3 to convert the delta(I) current into voltage.

The motivation and/or suggestion for doing so would have been to allow the Kimura circuit to be able to interface with another circuit which requires the input signal is a voltage signal instead of current signal.

As per claim 2, using a level shifter to shift the voltage at the common source node of an adder circuit is taught by Kimura in column 2, lines 51-55 (Fig. 1, transistors M55).

Response to Arguments

5. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

8/22/05

Minh Nguyen
Primary Examiner
Art Unit 2816